UNIVERSITÄT PADERBORN

Paderborn Center for Parallel Computing

NATIONALES HOCHLEISTUNGS RECHNEN

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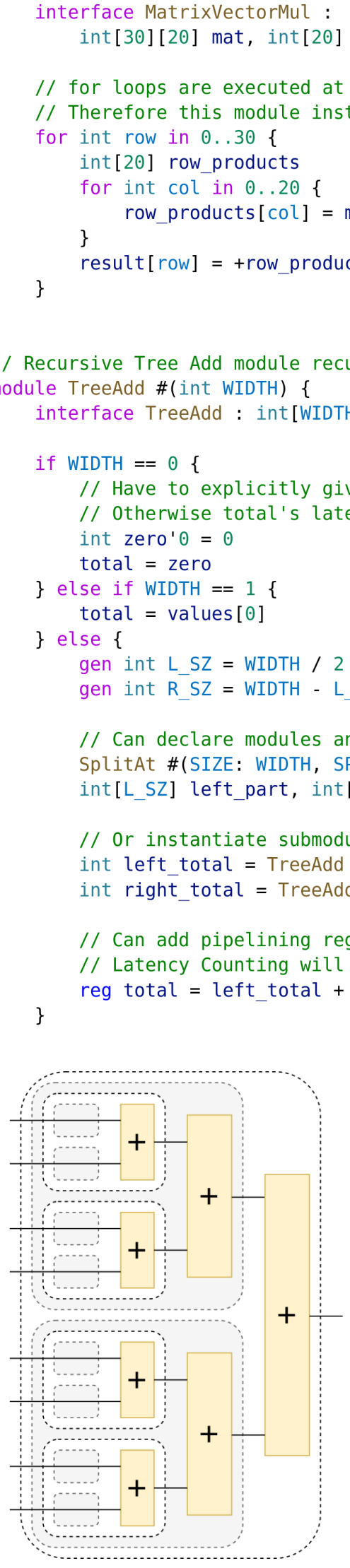
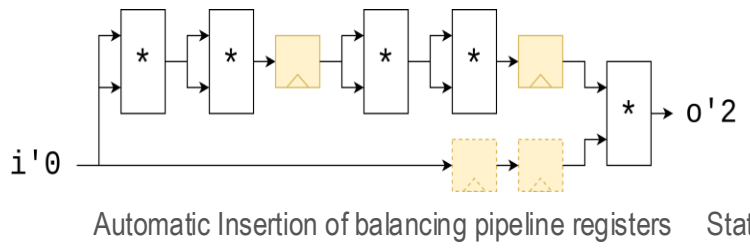
SIMPLIFYING HARDWARE DESIGN THROUGH SEMANTIC TIMING SUPPORT

Example SUS Code

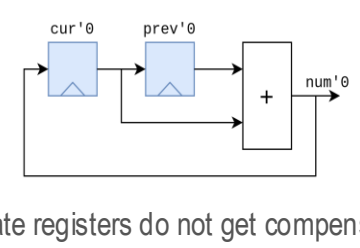
```
module MatrixVectorMul {
    interface MatrixVectorMul :
        int[30][20] mat, int[20] vec -> int[30] result

    // for loops are executed at compile time
    // Therefore this module instantiates 600 multipliers
    for int row in 0..30 {
        int[20] row_products
        for int col in 0..20 {
            row_products[col] = mat[row][col] * vec[col]
        }
        result[row] = +row_products
    }
}

// Recursive Tree Add module recurses smaller copies of itself.
module TreeAdd #(int WIDTH) {
    interface TreeAdd : int[WIDTH] values'0 -> int total

    if WIDTH == 0 {
        // Have to explicitly give zero a latency count.
        // Otherwise total's latency can't be determined.
        int zero'0 = 0
        total = zero
    } else if WIDTH == 1 {
        total = values[0]
    } else {
        gen int L_SZ = WIDTH / 2
        gen int R_SZ = WIDTH - L_SZ

        // Can declare modules and use them later.
        SplitAt #(SIZE: WIDTH, SPLIT_POINT: L_SZ, T: type int) split
        int[L_SZ] left_part, int[R_SZ] right_part = split(values)

        // Or instantiate submodules inline
        int left_total = TreeAdd #(WIDTH: L_SZ)(left_part)
        int right_total = TreeAdd #(WIDTH: R_SZ)(right_part)

        // Can add pipelining registers here too.
        // Latency Counting will figure it out.
        reg total = left_total + right_total
    }
}
```



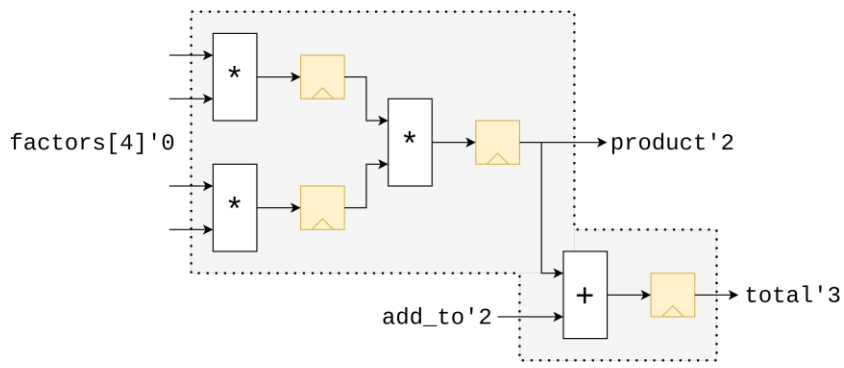
Pipelining through Latency Counting



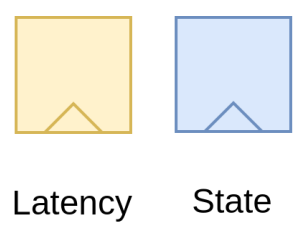
Automatic Insertion of balancing pipeline registers



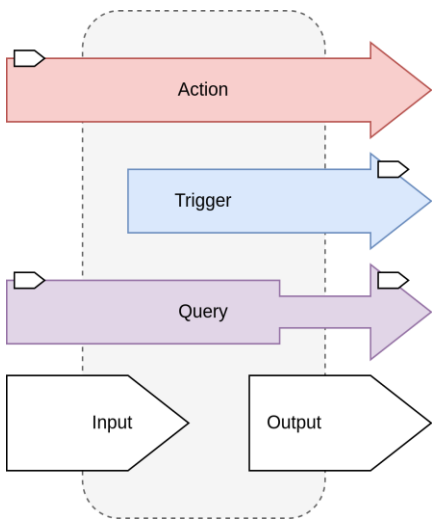
State registers do not get compensated

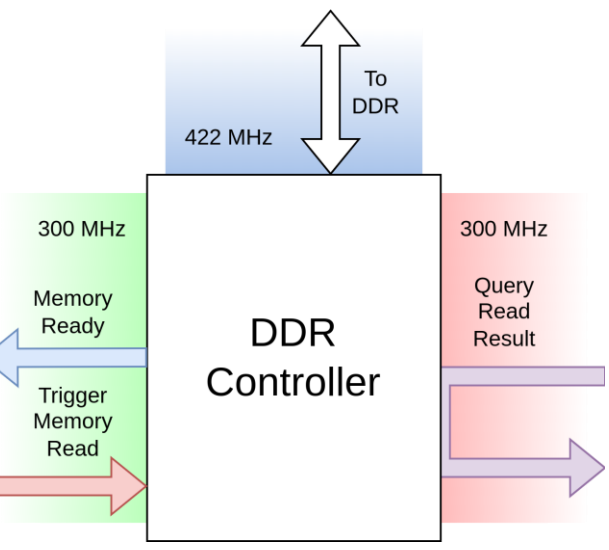


Input and output ports of modules have
"absolute latencies" inferred



Semantic wire relations in interface

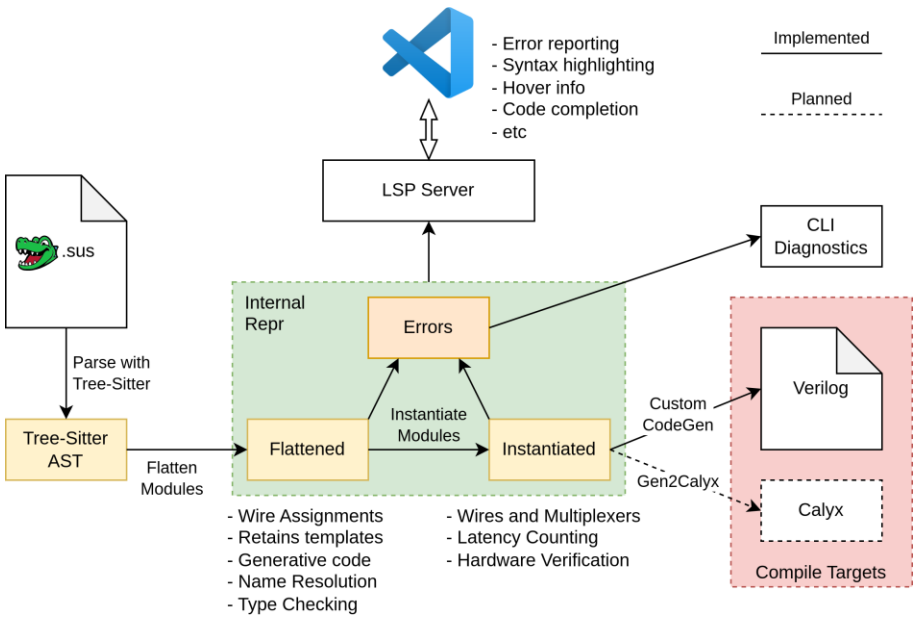




Actions, Triggers and Queries allow
Conditional presence of values to be expressed

Domains logically separate the wires of
Interfaces that aren't directly related in time
They also serve to support clock domains

Compiler Architecture



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