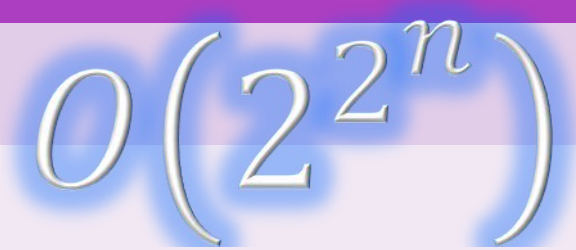
The 9th Dedekind Number

A case for FPGA Supercomputing

"The Nth Dedekind number is the number of Monotonic Boolean Functions in N variables"

D(0) =	2	Dedekind (1897)
D(1) =	3	Dedekind (1897)
D(2) =	6	Dedekind (1897)
D(3) =	20	Dedekind (1897)
D(4) =	168	Dedekind (1897)
D(5) =	7581	Church (1940)
D(6) =	7828354	Ward (1946)
D(7) =	2414682040998	Church (1965)
D(8) =	56130437228687557907788	Wiedemann (1991)
D(9) =	????	



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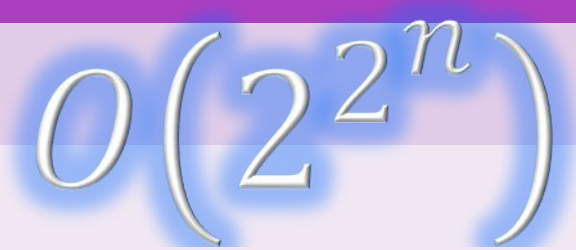
D(8) =	56130437228687557907788	Wiedemann (1991)
D(9) =	286386577668298411284691516675984988123 66	



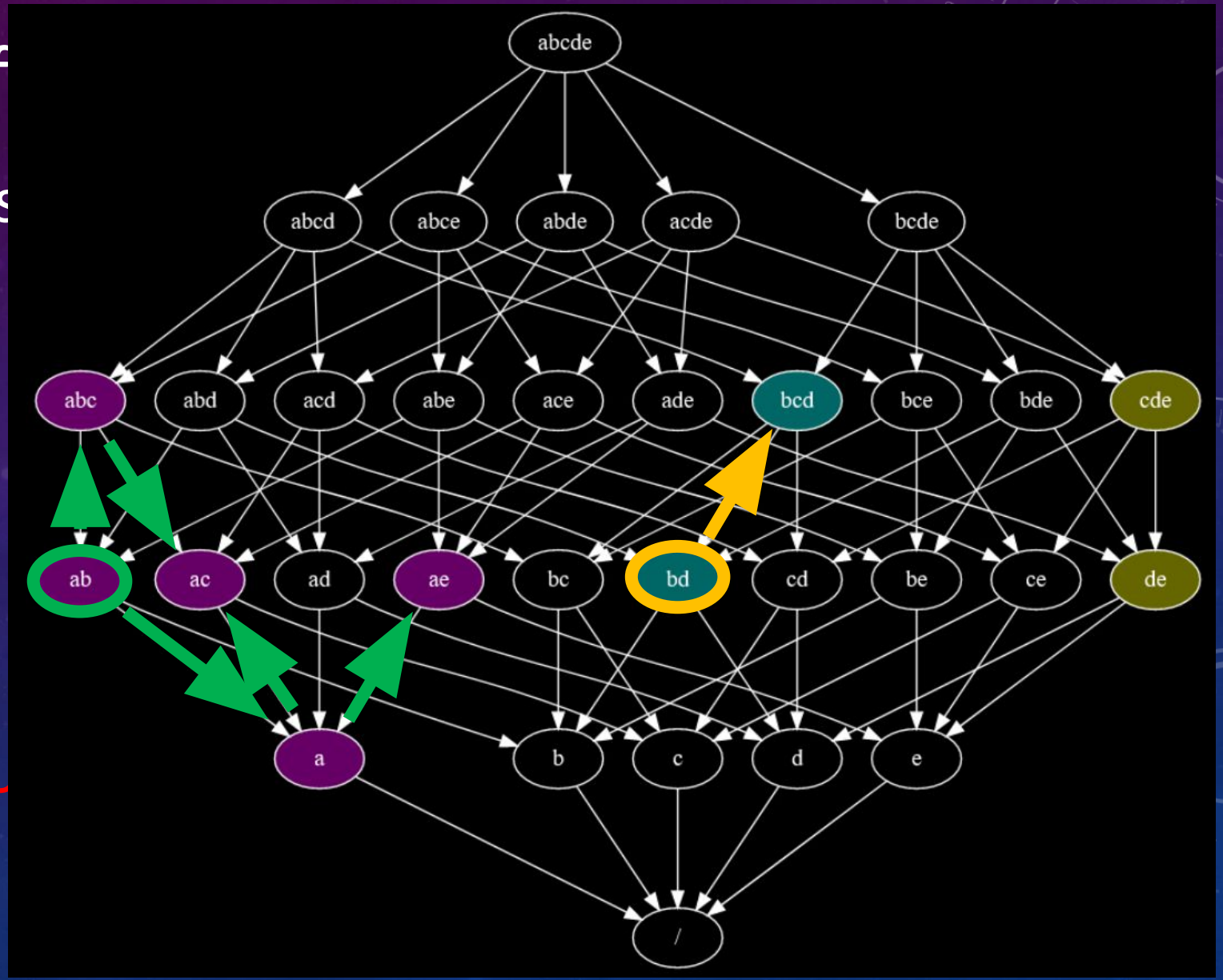
$$D(n+2) = \sum_{\substack{\alpha,\beta \in A_n \\ \alpha \leq \beta}} |[\bot, \alpha]| P_{n,2,\alpha,\beta} |[\beta, \top]|$$

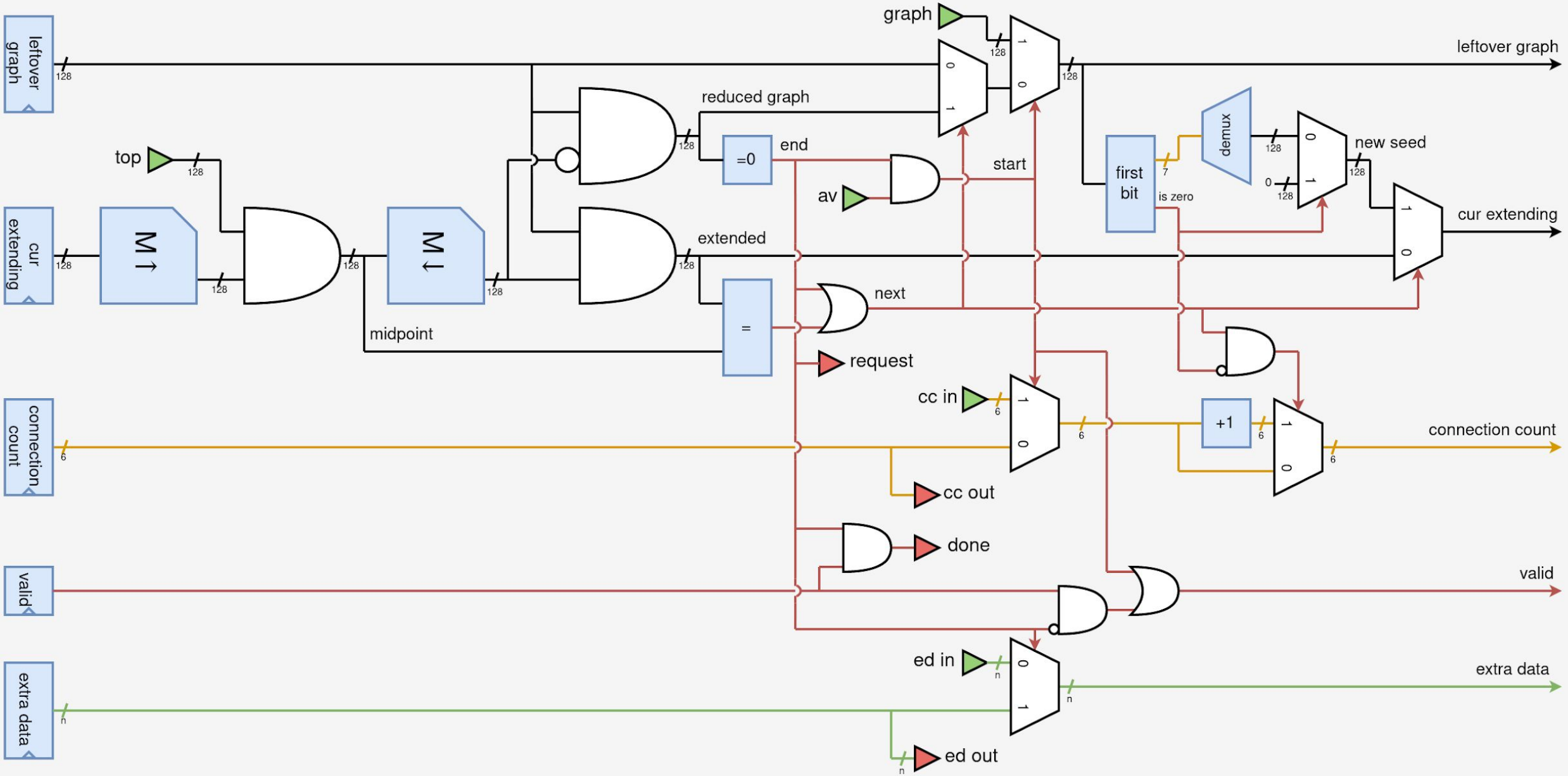
$1{,}148 * 10^{19}$ for D(9)

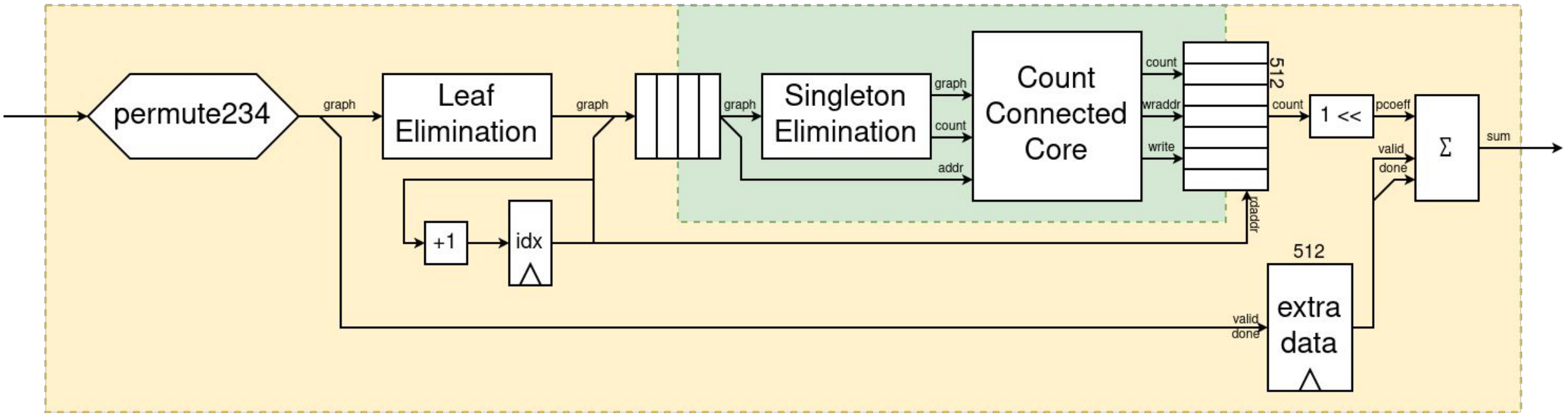
Computing P-Coëff

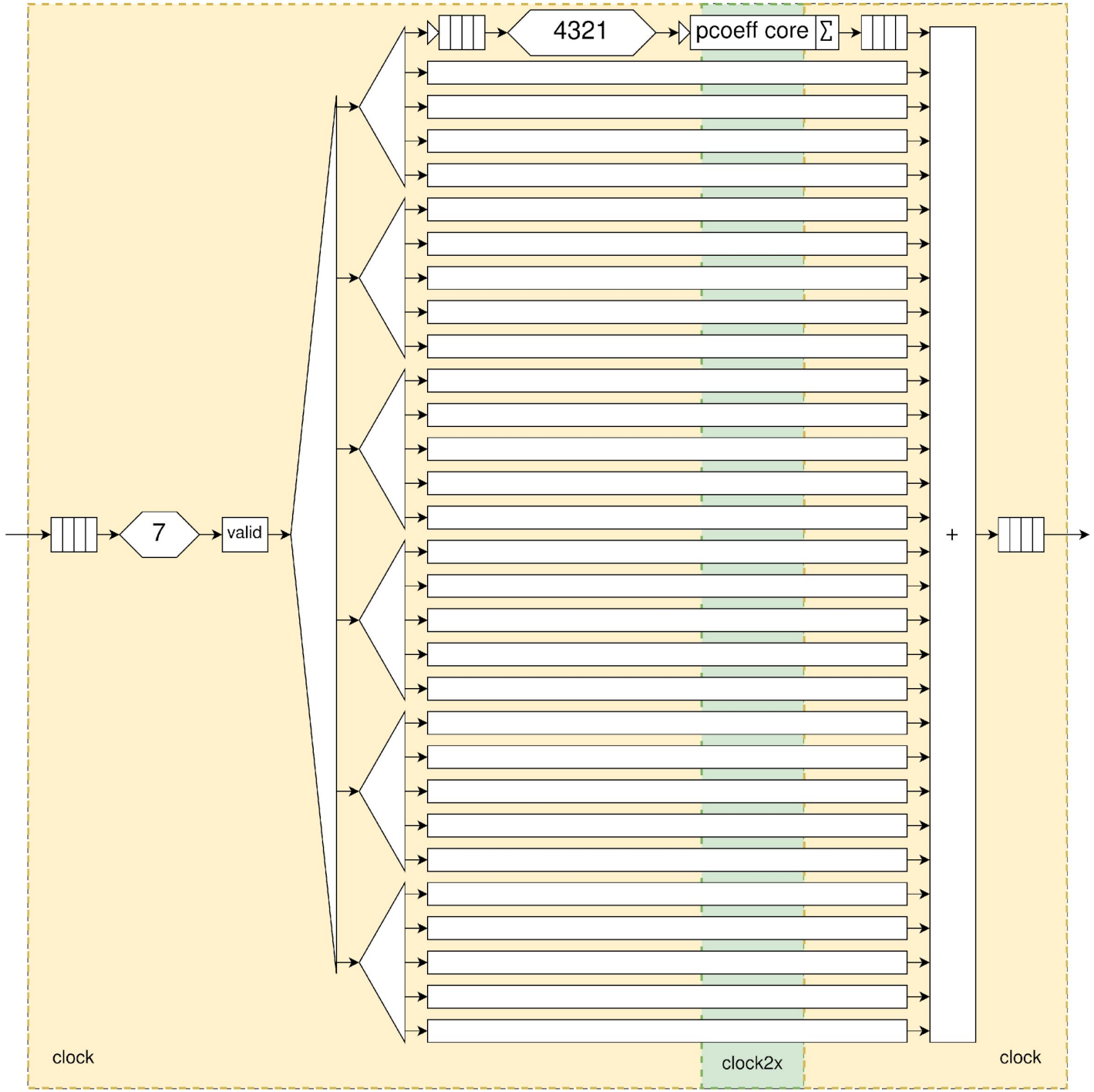
- Boolean Operations
- Fixed problem size
- Very branchy

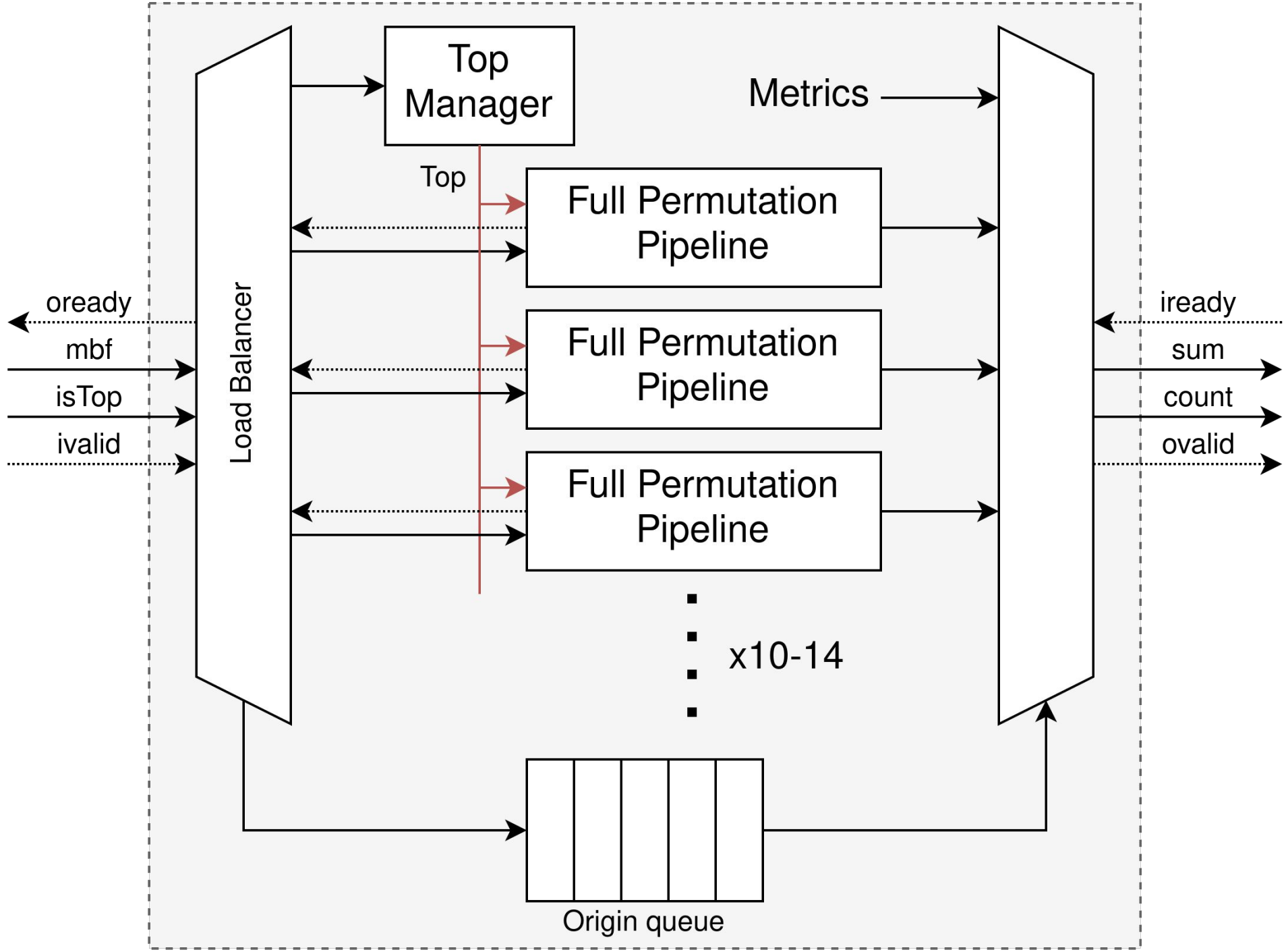
- Bad fit for CPU
- Can’t use SIMD
- Very bad fit for GPU
- Excellent for FPGA!




leftover graph
128
graph
128
leftover graph
reduced graph
top
128
=0
end
av
start
first bit
7
is zero
demux
128
0
128
new seed
128
cur extending
128
M→
128
M←
128
midpoint
extended
128
=
next
request
cur extending
cc in
6
+1
connection count
6
cc out
done
valid
valid
ed in
n
extra data
n
extra data
n
ed out

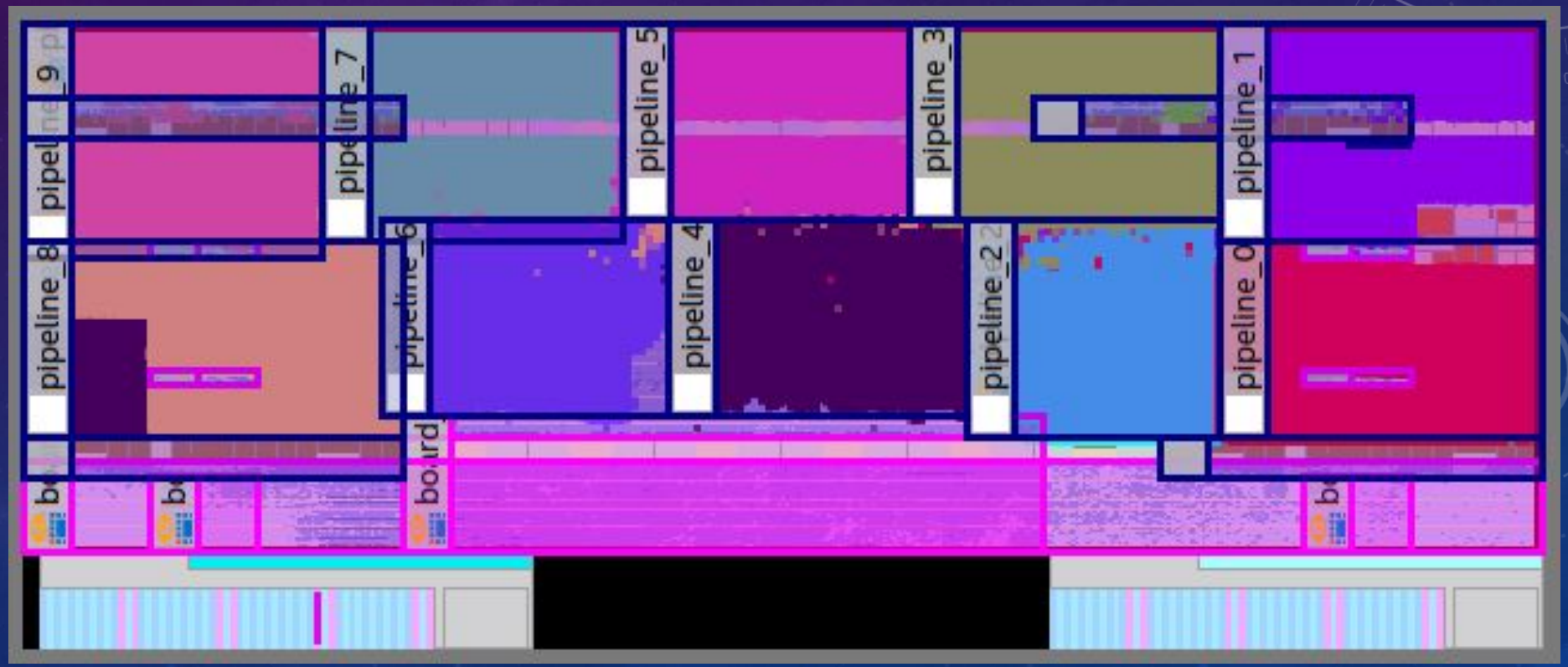

permute234
graph
Leaf Elimination
graph
graph
Singleton Elimination
graph
count
addr
Count Connected Core
count
wraddr
write
512
count
1 <<
pcoeff
valid
done
Σ
sum
rdaddr
+1
idx
512
valid
done
extra data

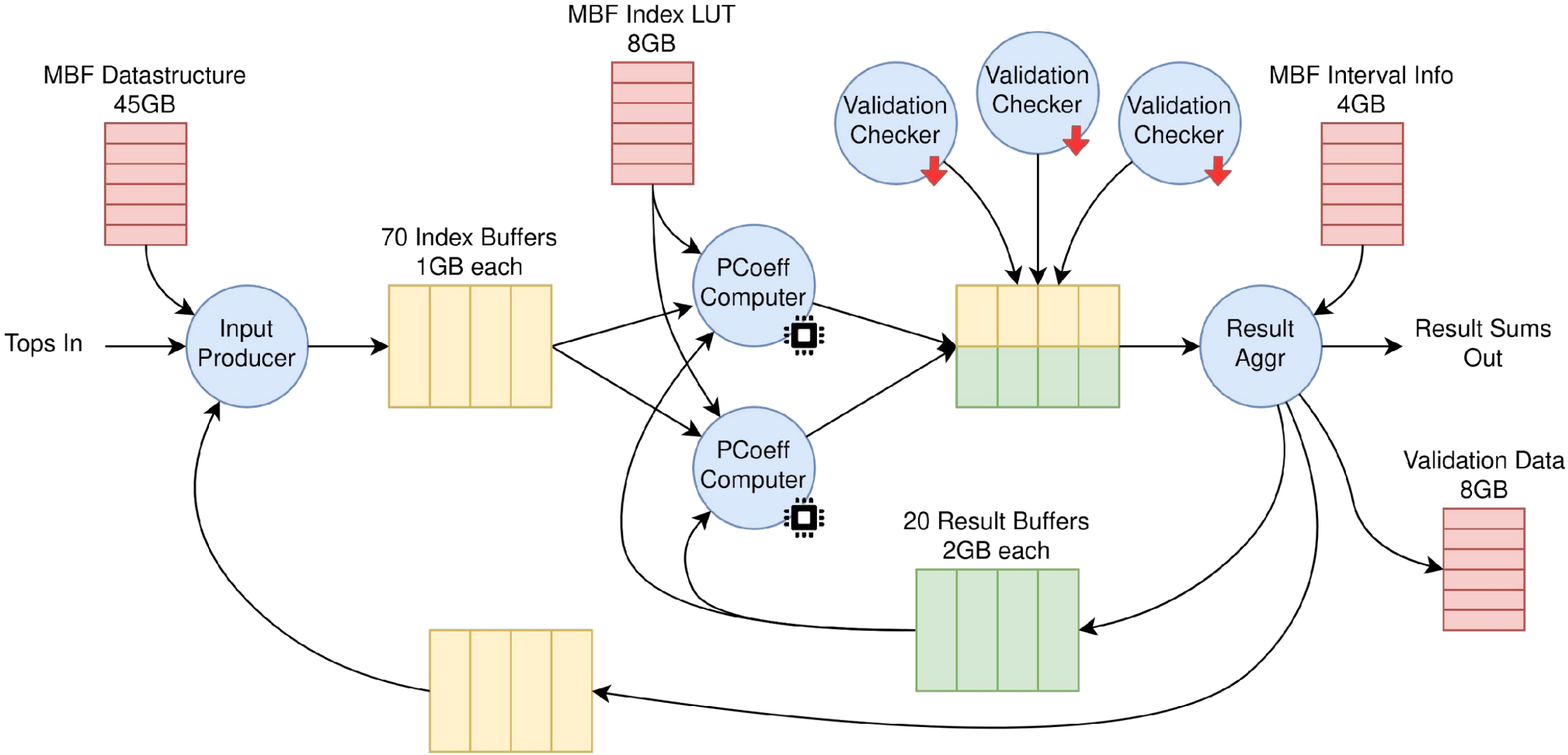

4321
pcoeff core
Σ
7
valid
+
clock
clock2x
clock


Top Manager
Metrics
Top
Full Permutation Pipeline
Full Permutation Pipeline
Full Permutation Pipeline
x10-14
Load Balancer
oready
mbf
isTop
ivalid
iready
sum
count
ovalid
Origin queue

FPGA Implementation

- 300 Count-Connected-Cores
- 450MHz
- ECC




MBF Index LUT
8GB
MBF Datastructure
45GB
Validation
Checker
Validation
Checker
Validation
Checker
MBF Interval Info
4GB
70 Index Buffers
1GB each
PCoeff
Computer
Tops In
Input
Producer
Result
Aggr
Result Sums
Out
PCoeff
Computer
Validation Data
8GB
20 Result Buffers
2GB each

Total project runtime

- FPGA 500x faster than AMD Milan CPU.
  - (usually ~40-60x)
- 15’000 100min jobs
- 4 months on Noctua 2

Should you use FPGAs for your project?

- Huge development cost
  - Designing HW is difficult
  - Testing HW is more difficult
  - 10-fold for native hardware!

hirtum.com/dedekind