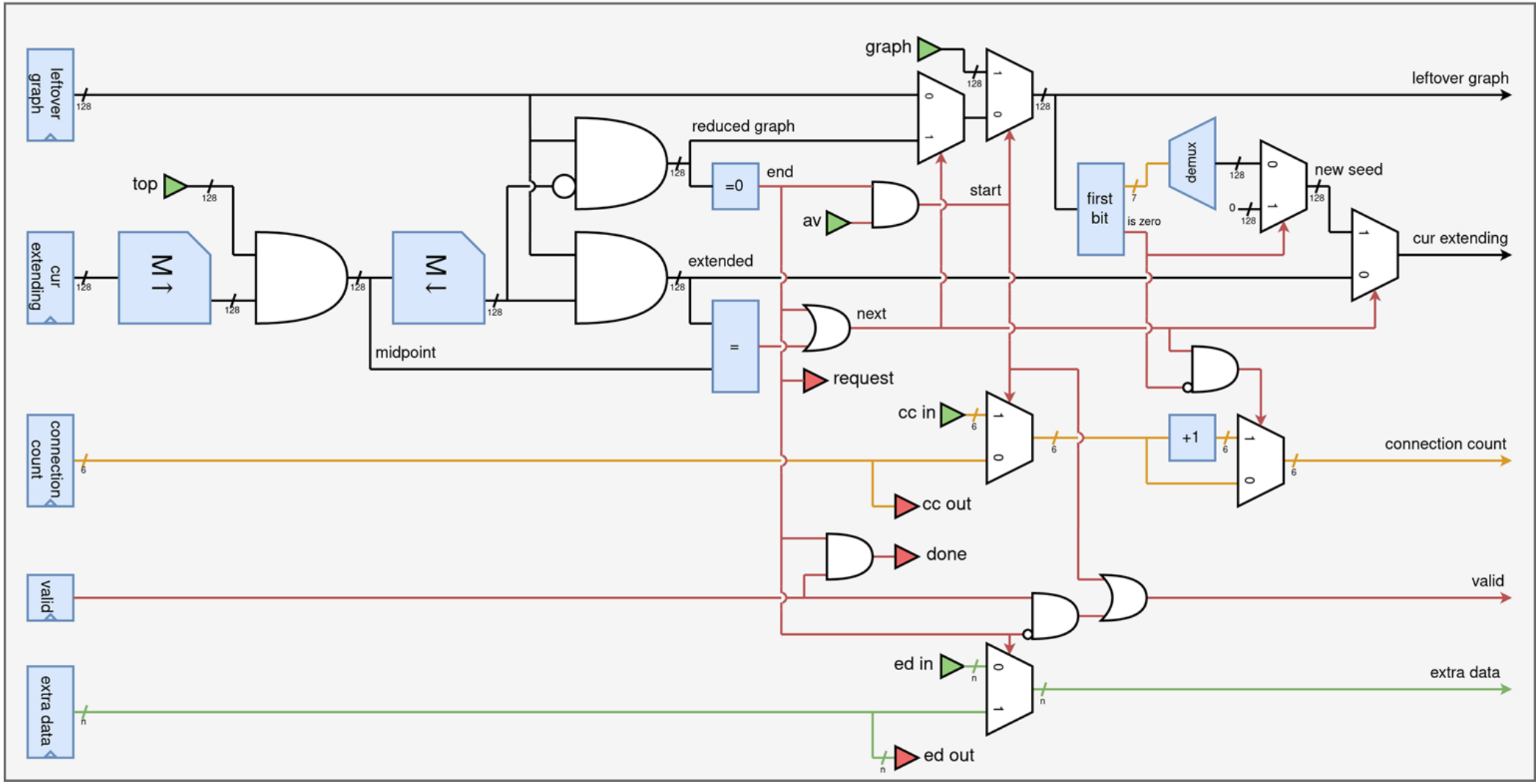
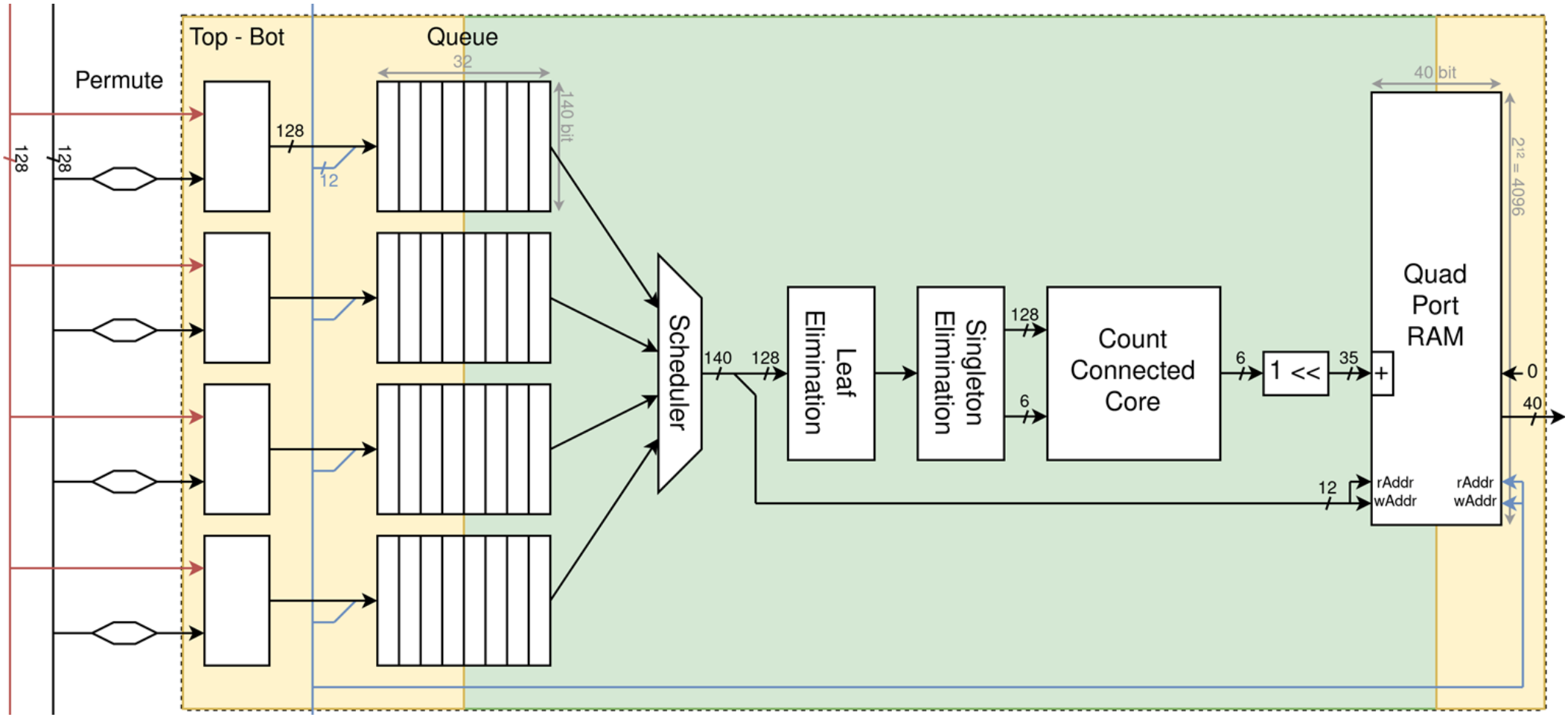
9th Dedekind Progress

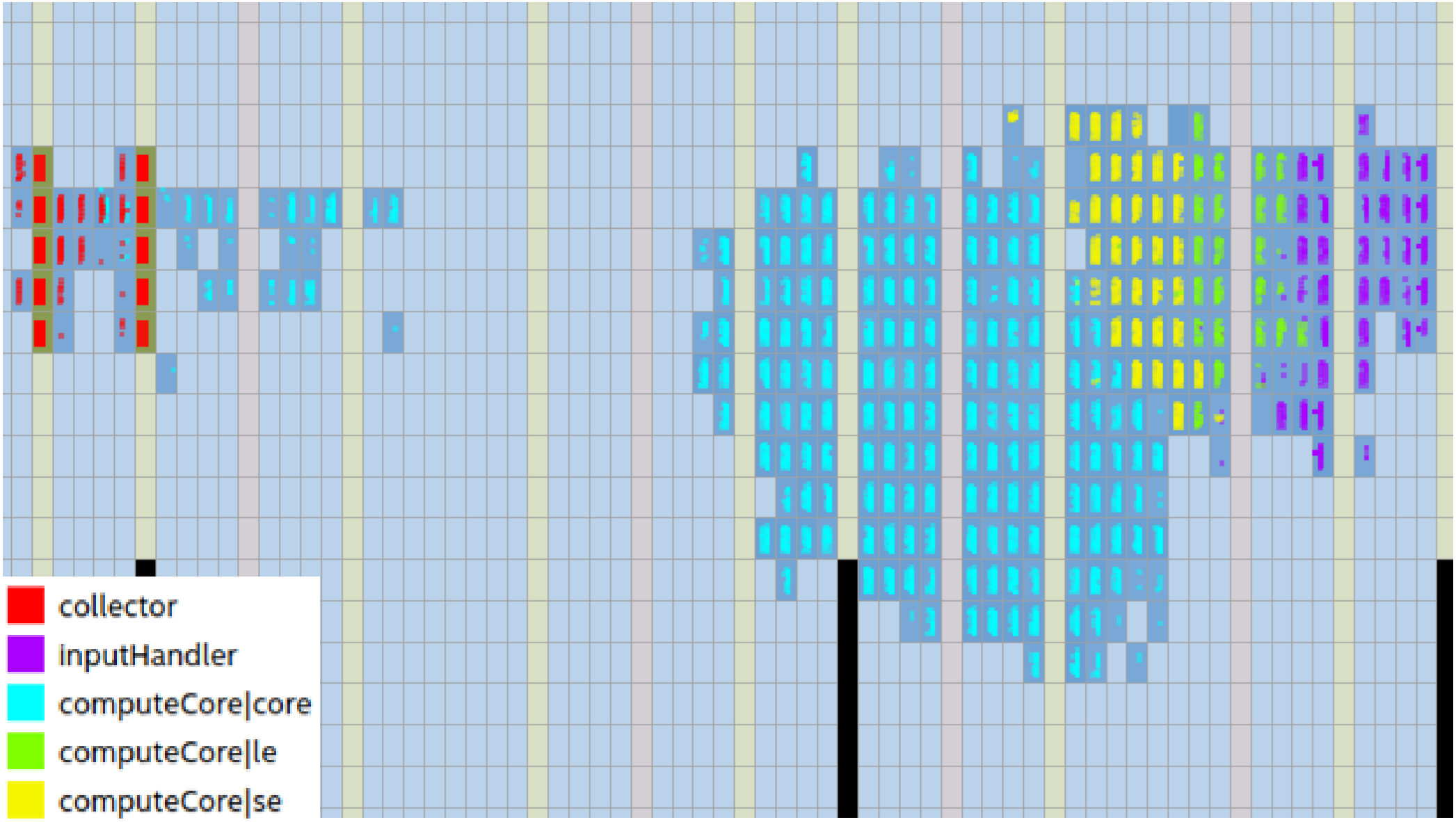
Pipelined CountConnected Core



Full Pipeline



Full Pipeline implemented



Resources and Fmax

Instance	Entity	ALMs needed [=A-B+C]
Stratix 10: 1ST040EH1F35E1VG		
fullPipeline		2101.4 (0.9)
collector	collectionModule	64.1 (23.4)
computeCore	computeModule	1770.2 (62.0)
core	pipelinedCountConnectedCore	1254.0 (10.8)
extraDataPipe	hyperpipeEnabled	12.0 (12.0)
graphAvalailbePipe	hyperpipeEnabled	1.2 (1.2)
le	leafElimination	177.4 (36.6)
se	singletonElimination	263.5 (110.4)
inputHandler	inputModule6	266.2 (0.3)

computeModule

Fmax	Restricted Fmax	Clock Name	Worst-Case Operating Conditions
801.92 MHz	801.92 MHz	pipelineClk	1 Slow vid1 0C Model

Changes compared to predictions

	Predicted	Implementation
ALMs/compute module	700	2100
Pipelines synthesizeable in 900’000 ALMs	1260	360
Fmax	500MHz	700MHz
Avg Cycles/Permutation	~5.074	~4.05
betas/second	493 million	246 million
FPGA Hours Required	25123	50354

FPGA Budget: 50000 hours!

Mathematical Developments

- Halving the total work:
  - Deduplication of α-β, β'-α' pairs.
  - 93 second D(8)

- Proof of D(9) evenness.
  - D(9) % 2 == 0

Where you come in

- Guidance and Advice:
  - How realistic is an Fmax of 800MHz?
    - Support on 520N cards?
      - Heat? Chip Speed Grade?
  - Full chip synthesis (Synthesize on Noctua?)
    - Pitfalls?
    - FPGA Initialization time?
    - FPGA Integrity checking after run?
  - OpenCL integration

End

(Also I still need that Quartus Licence)